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| **VZ\_\_C (CPU) Architecture (32/64 bit)** | |
| |  |  |  |  | | --- | --- | --- | --- | | **Opcode** | **Func** | **Name** | **Type** | | 00000 | 00 | ADD | R (IMM X) | |  | 01 | SUB |  | |  | 10 | AND |  | |  | 11 | OR |  | | 00001 | 00 | ADD-IMM | I | |  | 01 | SUB-IMM |  | |  | 10 | AND-IMM |  | |  | 11 | OR-IMM |  | | 00010 | 00 | MUL | R (IMM X) | |  | 01 | DIV |  | |  | 10 | XOR |  | | 00011 | 00 | MUL-IMM | I | |  | 01 | DIV-IMM |  | |  | 10 | XOR-IMM |  | |  | 11 | NOT |  | | 00100 | 00 | BRANCH-DIRECT | B | |  | 01 | BRANCH-SUBROTINE |  | |  | 10 | RETURN |  | | 00101 | 00 | BRANCH-INT EQUAL | BR | |  | 01 | BRANCH-INT NOT EQUAL |  | |  | 10 | BRANCH-FP EQUAL |  | |  | 11 | BRANCH-FP NOT EQUAL |  | | 00110 | 00 | BARNCH-INT >= | BR | |  | 01 | BRANCH-INT > |  | |  | 10 | BRANCH-INT <= |  | |  | 11 | BRANCH-INT < |  | | 00111 | 00 | BARNCH-FP >= | BR | |  | 01 | BRANCH-FP > |  | |  | 10 | BRANCH-FP <= |  | |  | 11 | BRANCH-FP < |  | | 01000 | 00 | LOAD-OFFSET-INT-32BIT | BR | |  | 01 | LOAD-OFFSET-INT-64BIT |  | |  | 10 | LOAD-OFFSET-INT-8BIT |  | |  | 11 | LOAD-OFFSET-INT-16BIT |  | | 01001 | 00 | LOAD-REG-INT-32BIT | B | |  | 01 | LOAD-REG-INT-64BIT |  | |  | 10 | LOAD-REG-INT-8BIT |  | |  | 11 | LOAD-REG-INT-16BIT |  | | 01010 | 00 | LOAD-OFFSET-FP-SINGLE | BR | |  | 01 | LOAD-OFFSET-FP-DOUBLE |  | | 01011 | 00 | LOAD-REG-FP-SINGLE | B | |  | 01 | LOAD-REG-FP-DOUBLE |  | | 01100 | 00 | STORE-OFFSET-INT-32BIT | BR | |  | 01 | STORE-OFFSET-INT-64BIT |  | |  | 10 | STORE-OFFSET-INT-8BIT |  | |  | 11 | STORE-OFFSET-INT-16BIT |  | | 01101 | 00 | STORE-REG-INT-32BIT | B | |  | 01 | STORE-REG-INT-64BIT |  | |  | 10 | STORE-REG-INT-8BIT |  | |  | 11 | STORE-REG-INT-16BIT |  | | 01110 | 00 | STORE-OFFSET-FP-SINGLE | BR | |  | 01 | STORE-OFFSET-FP-DOUBLE |  | | 01111 | 00 | STORE-REG-FP-SINGLE | B | |  | 01 | STORE-REG-FP-DOUBLE |  |   **INT/BASE Opcodes** | **INT/BASE Types**   |  | | --- | | **R-Type** | | |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | IMM | R2 | R1 | Rn | Func | Opcode | | 31 | 21 | 16 | 11 | 6 | 4 | | | **I-Type** | | |  |  |  |  | | --- | --- | --- | --- | | IMM | Rn | Func | Opcode | | 31 | 11 | 6 | 4 | | | **B-Type** | | |  |  |  |  |  | | --- | --- | --- | --- | --- | | IMM | R1 | Rn | Func | Opcode | | 31 | 16 | 11 | 6 | 4 | | | **BR-Type** | | |  |  |  | | --- | --- | --- | | IMM | Func | Opcode | | 31 | 6 | 4 | |   **INT/BASE Registers**   |  |  |  | | --- | --- | --- | | ZERO | 0 | Always Return 0 | | SP | 1 | Stack Pointer | | BACK | 2 | Subroutine Back Pointer | | R0~R28 | 3~31 | Program Register |   **Program Registers Rule**   |  |  |  | | --- | --- | --- | | R0~R7 | A0~A7 | Argument Register | | R8~R15 | N0~N7 | Return Register | | R16~R26 | T0~T9 | Temporary Register | | R27~R28 | K0~K1 | Kernel Register | |

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| **VZ\_\_C (CPU) Architecture (32/64 bit)** | |
| |  |  |  |  | | --- | --- | --- | --- | | **Opcode** | **Func** | **Name** | **Type** | | 10000 | 00 | F(S)ADD | R | |  | 01 | F(S)SUB |  | | 10001 | 00 | F(D)ADD | R | |  | 01 | F(D)SUB |  | | 10010 | 00 | F(S)MUL | R | |  | 01 | F(S)DIV |  | | 10011 | 00 | F(D)MUL | R | |  | 01 | F(D)DIV |  | | 10100 | 00 | F(S)POW | B | |  | 01 | F(S)SQRT |  | | 10101 | 00 | F(D)POW | B | |  | 01 | F(D)SQRT |  | | 10110 |  | RESERVED (FP) |  | | 10111 |  | RESERVED (FP) |  | | 11000 |  | RESERVED (STATUS) |  | | 11001 |  | RESERVED (STATUS) |  | | 11010 |  | RESERVED (STATUS) |  | | 11011 |  | RESERVED (STATUS) |  | | 11100 | 00 | SET MMU ADDRESS | I | |  | 01 | SET CURRENT PROCESS |  | | 11101 | 00 | GET INTERRUPT TYPE | I | |  | 01 | GET INTERRUPT ADDRESS |  | | 11110 | 00 | SET CPU MODE | I | |  | 01 | SET VIRTUAL MACHINE MODE |  | | 11111 | 00 | SYSTEM CALL | BR |   **FP/Status Opcodes** | **FP/Status Types**   |  | | --- | | **R-Type** | | |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | IMM | R2 | R1 | Rn | Func | Opcode | | 31 | 21 | 16 | 11 | 6 | 4 | | | **I-Type** | | |  |  |  |  | | --- | --- | --- | --- | | IMM | Rn | Func | Opcode | | 31 | 11 | 6 | 4 | | | **B-Type** | | |  |  |  |  |  | | --- | --- | --- | --- | --- | | IMM | R1 | Rn | Func | Opcode | | 31 | 16 | 11 | 6 | 4 | | | **BR-Type** | | |  |  |  | | --- | --- | --- | | IMM | Func | Opcode | | 31 | 6 | 4 | |   **FP Registers**   |  |  |  | | --- | --- | --- | | F0~F15 | 0~15 | Single/Double Floating-Point Register |   **STATUS Registers**   |  |  |  | | --- | --- | --- | | CPU MODE | X | 00 – All Access / 01 – KERNEL / 10 – DRIVER / 11 -USER | | VM MODE | X | VM Protect Mode activate when value is 1. | | INTR. TYPE | X | Interrupt Type | | INTR. ADDR | X | Interrupt Address |   **STATUS Opcode Operating Conditions**   |  |  | | --- | --- | | 11100 | When CPU Mode is 01 (KERNEL). | | 11101 | When CPU Mode is 01 (KERNEL), 10 (DRIVER). | | 11110 | When CPU Mode is 01 (KERNEL). | | 11111 | When CPU Mode is 10 (DRIVER), 11 (USER) | |

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| **VZ\_\_G (GPU) Architecture (32 bit)** | |
| |  |  |  |  | | --- | --- | --- | --- | | **Opcode** | **Func** | **Name** | **Type** | | 00000 | 00 | V.i16..ADD (Vector int16) | R | |  | 01 | V.i16..SUB (Vector int16) |  | |  | 10 | V.i16..MUL (Vector int16) |  | |  | 11 | OR |  | | 00001 | 00 | ADD-IMM | I | |  | 01 | SUB-IMM |  | |  | 10 | AND-IMM |  | |  | 11 | OR-IMM |  | | 00010 | 00 | MUL | R | |  | 01 | DIV |  | |  | 10 | XOR |  | | 00011 | 00 | MUL-IMM | I | |  | 01 | DIV-IMM |  | |  | 10 | XOR-IMM |  | |  | 11 | NOT |  | | 00100 | 00 | BRANCH-DIRECT | B | |  | 01 | BRANCH-SUBROTINE |  | |  | 10 | RETURN |  | | 00101 | 00 | BRANCH-INT EQUAL | BR | |  | 01 | BRANCH-INT NOT EQUAL |  | |  | 10 | BRANCH-FP EQUAL |  | |  | 11 | BRANCH-FP NOT EQUAL |  | | 00110 | 00 | BARNCH-INT >= | BR | |  | 01 | BRANCH-INT > |  | |  | 10 | BRANCH-INT <= |  | |  | 11 | BRANCH-INT < |  | | 00111 | 00 | BARNCH-FP >= | BR | |  | 01 | BRANCH-FP > |  | |  | 10 | BRANCH-FP <= |  | |  | 11 | BRANCH-FP < |  | | 01000 | 00 | LOAD-OFFSET-INT-32BIT | M | |  | 01 | LOAD-OFFSET-INT-64BIT |  | |  | 10 | LOAD-OFFSET-INT-8BIT |  | |  | 11 | LOAD-OFFSET-INT-16BIT |  | | 01001 | 00 | LOAD-REG-INT-32BIT | B | |  | 01 | LOAD-REG-INT-64BIT |  | |  | 10 | LOAD-REG-INT-8BIT |  | |  | 11 | LOAD-REG-INT-16BIT |  | | 01010 | 00 | LOAD-OFFSET-FP-32BIT | M | |  | 01 | LOAD-OFFSET-FP-64BIT |  | |  | 10 | LOAD-OFFSET-FP-8BIT |  | |  | 11 | LOAD-OFFSET-FP-16BIT |  | | 01011 | 00 | LOAD-REG-FP-32BIT | B | |  | 01 | LOAD-REG-FP-64BIT |  | |  | 10 | LOAD-REG-FP-8BIT |  | |  | 11 | LOAD-REG-FP-16BIT |  | | 01100 | 00 | STORE-OFFSET-INT-32BIT | M | |  | 01 | STORE-OFFSET-INT-64BIT |  | |  | 10 | STORE-OFFSET-INT-8BIT |  | |  | 11 | STORE-OFFSET-INT-16BIT |  | | 01101 | 00 | STORE-REG-INT-32BIT | B | |  | 01 | STORE-REG-INT-64BIT |  | |  | 10 | STORE-REG-INT-8BIT |  | |  | 11 | STORE-REG-INT-16BIT |  | | 01110 | 00 | STORE-OFFSET-FP-32BIT | M | |  | 01 | STORE-OFFSET-FP-64BIT |  | |  | 10 | STORE-OFFSET-FP-8BIT |  | |  | 11 | STORE-OFFSET-FP-16BIT |  | | 01111 | 00 | STORE-REG-FP-32BIT | B | |  | 01 | STORE-REG-FP-64BIT |  | |  | 10 | STORE-REG-FP-8BIT |  | |  | 11 | LOAD-REG-FP-16BIT |  |   **INT/BASE Opcodes** | **INT/BASE Types**   |  | | --- | | **R-Type** | | |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | IMM | R2 | R1 | Rn | Func | Opcode | | 31 | 21 | 16 | 11 | 6 | 4 | | | **I-Type** | | |  |  |  |  | | --- | --- | --- | --- | | IMM | Rn | Func | Opcode | | 31 | 11 | 6 | 4 | | | **B-Type** | | |  |  |  |  |  | | --- | --- | --- | --- | --- | | IMM | R1 | Rn | Func | Opcode | | 31 | 16 | 11 | 6 | 4 | | | **BR-Type** | | |  |  |  | | --- | --- | --- | | IMM | Func | Opcode | | 31 | 6 | 4 | |   **SIMD(Vector)/Scalar Registers**   |  |  |  | | --- | --- | --- | | ZERO | 0 | Always Return 0 | | SP | 1 | Stack Pointer | | BACK | 2 | Subroutine Back Pointer | | R0~R28 | 3~31 | Program Register | |